Precision Test Solutions To Maximize Yield and Reduce Catastrophic Risk In Today's Smaller Geometry ICs

KeyTek ESD & Latch-Up Test Systems
When Electronic Device Failure Is Not An Option

Increased integration of functionality on single, smaller geometry devices significantly increases the real risk of device failure due to ESD (Electrostatic Discharge). And it’s a fact: ESD hazards are a leading cause of device failure in the field today. This risk factor has widespread and potentially catastrophic implications; it can impact both product “time to market” cycles, as well as end-product reliability. If not addressed, these issues could result in severe financial consequences.

Experience the many benefits of working together with recognized experts in the field of ESD & Latch-Up testing. Our commitment to the discipline—and to the semiconductor industry—is wide ranging; we actively lead and participate on global standards committees and have helped define test methodologies to achieve regulatory standards and product quality objectives.

Our goal is to support you with lifelong service—from applications support, calibration services, and preventative maintenance to full technical field support.

Precision KeyTek semiconductor ESD & latch-up test systems can help you design and produce more reliable electronic products while achieving optimum IC production output. It’s what the market demands. And it’s a mission we share.

Minimize uncertainty. ESD and Latch-Up testing can be an arduous process. Defining quality standards and test methodologies for your devices. Determining the right systems to meet your parameters—both now and in the future. Rapid acquisition of the correct test systems to achieve your objectives. Maximizing yield critical to your success.

Thermo has your solution.

It begins with people of technology working with people of technology. Specialists understanding the challenges you face. Talking the same language. Rolling up our sleeves with you to solve the problem at hand. Questioning everything. And anticipating the consequences of every action we take. With fervor and commitment.

So if you’re a semiconductor quality professional, test engineer or device designer, let us help you achieve your goals with a solution tailored to your specific test requirements. Because by doing so, you’ll gain better control of your IC design and manufacturing process. You speed time-to-market cycles. And you take a proactive approach to reducing the uncertainty of semiconductor development and manufacturing.
**Best practices. Fulfilling expectations.** Today, Thermo has aligned its operations to focus on fully meeting—and exceeding—customer expectations at every level. And as technologies and regulatory issues evolve, to address change factors with responsive solutions. You only have to tour our manufacturing facility to understand how this commitment benefits our customers. And you’re invited.

What you’ll see is people driving technology. Translating “lean manufacturing” into customer-focused product development. And accepting the responsibility to make it happen, both rapidly and cost effectively. Building in quality throughout the process.

Understanding that it’s not just what you do, but what you don’t do that can mean the difference between success and “lost opportunity.” With all its ramifications.

Then, helping you to best utilize your test systems with applications support and training. And very importantly, responsive customer service. Transforming precision semiconductor test technology into indispensable productivity tools that optimize your capabilities and yield. And your return on investment.

You have expectations for your test systems and for your success. For the people at Thermo, it’s our business to fulfill them.

There’s always an appropriate and cost-effective test strategy to achieve yield objectives. It’s a fact. Rarely, however, does it identify itself.

But with the resources and expertise the people of Thermo bring to bear, together we’ll find it.

And in doing so, help take you, your organization, and its products to the next level of success.

**KeyTek ESD andLatch-Up Test Technology For Semiconductor Designers and Manufacturers**

As the semiconductor industry evolves to meet the requirements of today’s higher performance electronic products, advances in device geometries and I/C packages lead to increased sensitivity and susceptibility levels of individual devices to ESD (Electrostatic Discharge) events.

**Larger ICS. Smaller internal geometry. More integrated functions.** The fact is today many integrated circuits are getting larger; system-on-a-chip (SOC) is driving their internal geometry, and it is getting smaller. The demand for speed requires more function be integrated into a single device and better heat dissipation. Specialized devices are getting smaller and smaller in order to be used in very small products such as hearing aids, implantable drug infusion systems, and microelectronic-machines (MEMS).

The single most important issue related to managing the impact of ESD on devices and packages is the ability to test for the potentially destructive effects of ESD, identify, and then harden sensitive structures prior to full-scale production. This enables engineers and designers to make cost-effective and appropriate corrective actions in the development process, rather than after the fact.

Given the tremendously high cost of IC production, and today’s customer demands for precisely-timed component delivery schedules, an investment in the right ESD test system can rapidly return substantial dividends as a result of the time, material and lost opportunity costs it can save. With the smallest system footprints, lowest in-use-cost and highest installed base, Thermo Electron Corporation continues to lead the world with widely accepted “whole of test” solutions.

Thermo offers the correct KeyTek ESD and Latch-Up test system you require for every critical step of the semiconductor design and manufacturing process.
Simplified Silicon Integrated Circuit Production

- Integrated Circuit Analysis and Simulation
  - KeyTek MK.2
  - KeyTek RCDM3
  - KeyTek TLP

- Wafer Functional and Electrical Performance Verification
  - KeyTek TLP

- Electronic Circuit Functional Creation (Deposition)

- Raw Wafer Production

- Silicon Ingot Production

- Product Field Return

- Packaging and Quality Control
  - diced Packaging
  - Attach leads Encapsulation
  - Device Final Test
  - Quality Control

- Market
Relay-Based Operation With 128, 256, 384, 512, or 768 Pin Test Capabilities

The KeyTek ZapMaster® Mk.2 has been developed in response to global market demands for products that are smaller, faster, and smarter.

A turnkey, field upgradeable test system, the KeyTek ZapMaster Mk.2 test system allows you to test your devices for ESD and Latch-Up susceptibility from the design phase through the post-production qualification stage in an efficient and cost-effective manner.

Building on legendary performance and reliability. The KeyTek ZapMaster Mk.2 has been designed and developed based on the heritage of the testing reliability, accuracy and durability of the original KeyTek ZapMaster. In constant testing use since the late-eighties, the KeyTek Zapaster has been embraced by leading manufacturers around the world, with an installed user base that numbers well into the hundreds.

Features

- Test devices up to 768 pins; systems avaiable configured as 128, 256, 384, 512 or 768 pins.
- Compatible with ALL 256 pin KeyTek ZapMaster test fixtures when equipped with the optional Mk.2 to ZapMaster Carrier, and ALL Verifier DUT fixtures when equipped with the optional Mk.2 to Verifier DUT adapter. (Both cases require the system be configured with 512 or 768 pins.)

- Human Body Model (HBM) per ESDA STM5.1, J EDEC EIAJ ESD22-A114, MIL-STD 883E and AEC Q100-002 specifications, 50V to 8KV.
- Machine Model (MM) per ESDA STM5.2, J EDEC EIAJ ESD22-A115, and AEC Q100-003, 50V to 2KV.
- Latch-Up testing per J EDEC EIAJ ESD 78 and AEC Q100-004 including preconditioning, state read-back and full control of each test pin.
- Pin Drivers for use during Latch-Up testing and parametric measurements:
  - Vector input capability from standard tester platforms,
  - 64k vectors per pin with read-back, and;
  - Up to 10MHz vector rate programmable from an internal clock to quickly set the device into the desired state for testing.
- Up to six separate V/I supplies for DUT power, curve tracing, and latch-up stimulus with 4-wire sensing at the DUT board for high accuracy. System design also provides high current capability directly through the V/I matrix.
- Multiple self-test diagnostic routines to ensure system integrity throughout the entire relay matrix, right up to the test socket.
- Test reports include pre-stress, pre-fail (ESD) and post-fail data, as well as full curve trace and specific data point measurements. Data can be exported for statistical evaluation and presentation.
- Individual pin parametrics allow the user to define V/I levels, compliance ranges, and curve trace parameters for each pin individually.
- Reliable, relay-based operation that enables test speeds that are 5 to 10* times faster than robotic mechanical driven testers. This can dramatically reduce device qualification time.

And, while test protocols will largely dictate test speeds, the KeyTek ZapMaster Mk.2 provides 8 DUT (device under test) test capability (total of 8, 16 pin DUT's when configured with 128 pins, DUT pin count increases with system pin count), which can substantially increase testing throughput.

* When compared to existing robotic mechanical devices. Test protocol may limit test speeds.
Rapid, Easy-To-Use Testing Operations

- Control by the Windows®-based software is both intuitive and comprehensive.

- Allows tests to be set up quickly, and helps keep operator and programmer training to a minimum.

- A powerful embedded VME controller, capable of handling an enormous amount of test program and result data, controls the system hardware.

- Eliminates unnecessary data transfer and increases throughput, a real time-saver when evaluating large devices.

Consistent, Precise ESD Waveforms

By locating multiple discharge networks close to the test fixture board itself, unwanted stray inductance and capacitance is kept to a minimum at every pin. This insures:

- Excellent waveform quality, and;

- Highly repeatable and reproducible test data.

KeyTek ZapMaster Mk.2 ESD Test Capabilities

- Human Body Model (HBM) and Machine Model (MM) testing to the most prevalent industry standards.

- Latch-Up Testing Per J EDEC’s EIA/J ESD 78 Method (when equipped with the Pin Drivers option).

- Equipped with Voltage and Current (V/I) power supplies, each of which has a wide dynamic range enabling them to force and measure signals spanning from the milli-volt and nanoamp range, up to 100 volts and 10 amps. Provides a fast and versatile means of making any number of DC parametric leakage measurements and Latch-Up tests, while offering total control and protection of the DUT. (Additional V/I supply configurations are also available.)

- Advanced device preconditioning capability. The preconditioning option allows the DUT to be vectored with complex test and vector patterns, which gives the test operator excellent experimental tools and full production test control over the DUT. Each device pin can be driven with vectors up to 64k deep, at selectable speeds of up to 10MHz, and with the read back capability on every pin, and device state, comprehensive state verification is fast and easy.

- Switching matrix provides consistent and repeatable ESD paths; also allows any pin to be grounded, floated, vectored or connected in any order, to any of the installed pulse sources or V/I supplies (a maximum of 5 DUT V/I’s are available for biasing).

Define, achieve and sustain your component reliability objectives - today and tomorrow. Custom configuration options enable you to purchase a system to meet your initial test needs and budgets. Then, when corporate or industry standards demand test systems to be upgraded, it can be done at your site to minimize down time and eliminate the need and expense of shipping the unit back to the factory.

The need to meet future industry test standards is always a concern when evaluating test systems, but due to the system’s flexible modular design, meeting these standards in the future will be easier and very cost effective.

Available options include: additional pins, V/I supplies, high speed vectoring capabilities, test features and pulse sources.

Super fast, reliable & compact ESD and Latch-Up Test System enables you to accelerate ESD & Latch-Up test speeds—in just 4 square feet of floor space.
Reproduces Real World CDM Events

The KeyTek RCDM3 is a fully-automated, PC-controlled system that enables the user to test devices and identify potential Charged Device Model (CDM) ESD failure problems prior to the release of a device for production.

The KeyTek RCDM3 meets the two dominant CDM test methods, and can be ordered with either or both of these standards:

- ESDA STM 5.3.1
- JEDEC, JESD22-C101

For a robotic CDM test, the device is generally charged in an electric field by placing the device between a charged surface and a ground plane. The discharge is performed by bringing a grounded discharge pin into contact with one of the pins of the charged device. The device then rapidly discharges and the process is repeated for other pins under test.

In the KeyTek RCDM3, an event detector ensures that each pin is discharged, ensuring proper alignment and contact between the device and the system pin. The event detector illuminates a lamp on the system and displays a symbol on the system controller video display each time a CDM event occurs. The events are logged in the software and reported at the completion of the test, providing the user with confirmation that all pins are being discharged properly during the test. Any non-stressed pins are identified and can be targeted for retesting.

Because of the potentially destructive nature of a CDM event, manufacturers demand easy and accurate test configuration to allow efficient device characterization. With the proliferation of device types and requisite tests, it’s critical that the testers enable operators to quickly get new device tests up and running. The KeyTek RCDM3 offers unique features to ensure the fastest set-up and test throughput available.

The KeyTek RCDM3 is the only tester with three independent cameras to allow fast, precision alignment of a new device, and thereby ensuring the operator is running tests quickly and efficiently.

The Charged Device Model. In the 1970’s, design and test engineers began testing devices to well defined ESD pulses thought to be representative of human discharges (Human Body Model, or HBM) and of discharges from other items (Machine Model, or MM). Thermo, a pioneer in ESD test technology, participated with industry organizations to develop appropriate ESD test protocols that would allow standards to be used effectively throughout the entire semiconductor industry. However, these tests were not sufficient to determine the ability of a device to withstand the effects of the device becoming charged during handling, and then quickly discharged when coming in contact with a metal handler, or any surface at a different potential.

During handling, a semiconductor package can become charged and that charge is triboelectrically coupled to the internal structure of the device. If the package or any of its pins come into contact with a metal surface, the device will discharge in picoseconds, with peak currents on the order of 10's of amps; a potentially destructive ESD event.
Features

- A self-contained turnkey system.
- Charged Device Model testing per J EDEC Standard J ESD22-C101, with full user control of all stress levels and polarities (RCDM-J EDEC).
- Charged Device Model testing per ESDA STM 5.3.1 specification, with full user control of all stress levels and polarities (RCDM-ESDA).
- Three camera configuration provides easy pin positioning for rapid device set-up and programming. Once package outlines are programmed, they can be easily saved for future retrieval. Orthogonal views with wide view and close-up screens provide easy pin location.
- Built-in vacuum device hold down system which makes device positioning fast and accurate; also enables the testing of devices of virtually any size or configuration.
- Built-in waveform monitor facilitates oscilloscope monitoring of the discharge pulse for waveform verification purposes. Calibration of the high voltage power supply is made simple via a software routine and a test point located on the front panel (where a convenient wrist strap ground point is also located).
- Test devices of any configuration; device geometry is virtually unlimited including stab and smart cards.
- Direct Charge method charges the DUT through a selected pin, then discharges that pin and/or the selected pins sequentially, via the discharge probe to ground. The user has full control of the pins to charge and discharge.
- Field-Induced Charge method elevates the entire DUT to the selected voltage by charging the isolated charge plate, which the device is located on. Then the selected pin is discharged via the discharge pin to ground. The user has full control of the pins to charge and discharge.
- Windows®-based application software provides a user-friendly interface for device definition, test plan generation and DUT orientation.
- Pre-defined pin map screens facilitate pin location. Only a few pins need to be located to define the entire device.
- Zap detection circuit for confirmed discharge event.
- Totally enclosed test chamber allows convenient connection to test in inert gas atmosphere.
- System interlocks interrupt the internal tester movement—as a safety precaution for both the operator and DUT (Device Under Test). In the event of an emergency, a stop switch is located within easy reach for immediate system shut down.

Designed For Years of Dependable Service. The KeyTek RCDM 3 test system has been designed to accommodate testing of virtually any size device package. A complete, value-packed system, the KeyTek RCDM 3 will be an indispensable testing tool for years to come, particularly as device package geometries become smaller and more powerful.

It requires only an oscilloscope (not included) to perform comprehensive Robotic CDM testing; all other equipment, and Windows®-based software is included, eliminating the need for future capital outlays for upgrades.
A Breakthrough In High Bandwidth ESD Stress Simulation

The KeyTek Eclipse VF-TLP transmission line pulser is the world’s first “high bandwidth” pulse curve tracer. A turnkey high power Time Domain Reflectometer, it facilitates engineering evaluation of semiconductor structures under dynamic stresses.

A flexible interactive design tool, the KeyTek Eclipse VF-TLP provides multiple threat simulation—HBM, Fast HBM and CDM—at package and wafer levels. It provides ESD failure thresholds and detailed ESD protection structure information to allow the designer to characterize the robustness of the design in a real world environment.

The KeyTek Eclipse features the True Time Domain (TDR) measurement method. This enables future parameter extraction and accurate multiple threat simulation. It also displays test environment feedback.

CDM simulation capability enables complete device stress simulation; probing for weakness and permitting designers to test cutting edge “ultra-fast” protection structure design.

The system incorporates a highly intuitive user interface with time saving automation of test tasks. All system parameters, measurements and results are displayed graphically and results can be simply exported for inclusion in test reports. Calibration methods are easy and convenient.

The KeyTek Eclipse VF-TLP shortens the protection structure design evaluation/performance evaluation cycle and speeds and gives device designers the confidence to publish their devices to corporate functional libraries, while reducing costly scraping of early device runs (WIP).

An easily configured system, it is compact, fast, and accurate and enables you to flawlessly execute tests to ensure greatest yield.

KeyTek Eclipse VF-TLP Systems

Eclipse Alpha. An entry-level turnkey system, with HBM and Fast HBM capability.

Eclipse Gamma and Eclipse Epsilon. More highly capable allowing faster event simulation required by the CDM event and offering information that can assist in device parameter extraction.

When configured with user-supplied equipment, KeyTek Eclipse VF-TLP testers facilitate enhanced and cost-effective test capability.

Features

• TrueTime Domain (TDR) measurement method.
• Comprehensive calibration methodology.
• Integrated device leakage and curve tracing.
• Optional TDRT and Current Probe mode available.
• Simulates HBM, real HBM and CDM events.
• True positive and negative polarities.
• Ultra “clean” pulses.
• Comprehensive Data evaluation tools.
• Accurate 50 Ω system impedance.
• High test throughput.
• Complete device failure characterization.
• Biased and non-biased pulsing.
• High Peak current, 5 A (into 50 Ω), 10 A into short circuit.
• Packaged 48 pin device fixture included.

KeyTek Eclipse VF-TLP

An easily configured test system simulating Human Body Model (HBM), real HBM and Charged Device Model (CDM) threats.
Single Source, Total Semiconductor ESD & Latch-Up Test Solutions.

Specialists who understand the challenges you face. Innovative ideas. Leading technologies. Breadth of high yield semiconductor test equipment. Thermo—your semiconductor test solutions partner. Contact us today for details.